Claims

1. A substrate for flip chip packaging, comprising:

a multiple layer substrate having a first layer forming a signal plane and second and third layers beneath said first layer, said second and third layers forming selectively power and ground planes;

power, ground and signal bump pads on said first layer, said power and ground bump pads extending in parallel rows in a designated position; and

microvias connecting said power bump pads directly to said power plane and said ground bump pads directly to said ground plane.

2. A substrate as claimed in claim 1, including a further signal plane below said power and ground planes, and microvias connecting related signal bump pads on said first layer to said further signal plane.

3. A substrate as claimed in claim 1, said first layer on a top surface of said substrate.

4. A substrate as claimed in claim 2, said further signal plane on a bottom surface of said substrate.

5. A substrate as claimed in claim 1, said signal bump pads extending in parallel rows; said rows of signal power and ground bump pads positioned sequentially in the order of positioning of said signal, power and ground planes.

6. A flip chip package comprising a flip chip mounted on a multistage substrate having a first, signal, layer, a power layer having a power plane, and a ground layer having a ground plane beneath said signal layer;

power, ground and signal bump pads formed on said first layer, said power and ground bump pads extending in parallel rows in a designated position;

microvias connecting said power and ground bump pads directly to said power and ground planes;

power and ground bumps on said flip chip, extending in parallel rows in a designated position, and connected to said power and ground bump pads;

signal bumps on said flip chip connected to said signal bump pads.

7. A flip chip package as claimed in claim 6, including a further layer forming a further signal plane beneath said power and ground planes, and microvias connecting signal bump pads on said first layer to said further signal plane.

8. A flip chip package as claimed in claim 6, said first layer on a top layer of said substrate.

9. A flip chip package as claimed in claim 7, said further signal plane on a bottom surface of said substrate.

10. A flip chip package as claimed in claim 6, said signal bump pads extending in parallel rows, said rows of signal, power and ground bump pads positioned sequentially in the order of positioning of said signal power and ground planes.

11. A method of making a substrate for flip chip packaging, comprising:

forming signal, power and ground planes at various layers of a multistage substrate;

forming power and ground bump pads on a top layer of said substrate, said bump pads extending in parallel rows at a designated position; and,

forming microvias to connect said power bump pads directly to said power plane and to connect said ground bump pads directly to said ground plane.

12. A method as claimed in claim 11, including forming signal bump pads, extending in rows parallel to said power and ground bump pad rows, said rows of signal, power and ground bump pads formed sequentially in the order of positioning of said signal, power and ground planes.

13. A method as claimed in claim 11, wherein the method is implemented in part on a processor forming part of a computer system.

14. A method as claimed in claim 12, wherein the computer system provides data for a layout for a substrate for flip chip packaging, the data indicative of the layout and for use in manufacturing of the substrate for flip chip packaging.

15. A machine readable storage medium comprising a plurality of instructions stored therein for performing the steps of:

forming representations of signal, power and ground planes at various layers of a virtual multistage substrate;

forming representations of power and ground bump pads on a top layer of said substrate, said bump pads extending in parallel rows at a designated position;

forming representations of microvias to connect said power bump pads directly to said power plane and to connect said ground bump pads directly to said ground plane and,

providing the representations in a format for use in a manufacturing process to produce to produce a product based on the representations.

16. A machine readable storage medium as defined in claim 15 comprising:

a computer for reading the machine readable storage medium and for performing the instructions stored therein.

17. A machine readable storage medium as defined in claim 16 comprising:

a manufacturing system responsive to a representation received from the computer for producing a flip chip package in accordance with the representation.